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PORTLAND, OREGON 97208-2786 PORTLAND, OREGON 97202-5936
U.S.A.

JAMES H. WALTERS*
JOHN P. DELLETT*
OF COUNSEL

TELEPHONE
(503) 224-0115
FAX
(503) 224-7017
peter.ts@onemain.com
* Registered Patent Attorney

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In re Application of | Confirmation No.: 1735

Stan W. BOWLIN | Art Unit: 2189

S. N. 09/675,974 | Examiner: C. E. Lee

Filed: 09/29/00

For: METHOD AND APPARATUS FOR RAPID DATA TRANSFER BETWEEN DISSIMILAR DEVICES

REPLY BRIEF ON BEHALF OF APPELLANT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the Examiner's answer mailed August 19, 2004, applicant respectfully submits this reply brief.

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STATUS OF CLAIMS

Claims 1-19 are pending in the application, are rejected, and are the claims under appeal. Appellant wishes to prosecute this appeal with respect to claims 1-19. An appendix of claims is included herewith.

This application was originally filed on September 29, 2000, with claims 1-9. A first office action was mailed February 12, 2003, and a response to that action was filed June 8, 2003, amending claims and adding new claims. A final office action was mailed August 11, 2003, and a response after final was filed November 12, 2003. The Examiner issued an advisory action November 26, 2003, maintaining the rejections, but noting that amendments after final would not be entered for purposes of appeal. Applicant filed a notice of appeal by fax on January 11, 2004, to which this present appeal brief relates.

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GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The broad issue presented in this appeal is whether the Examiner's final rejection of claims 1-19 is proper. The issue may be stated more narrowly as:

1. Whether claims 1-19 are unpatentable under 35 U.S.C. 112, first paragraph, because the specification is not enabling for transferring a unit of data on a bus from a source to at least two destinations substantially simultaneously.

2. Whether claims 10 and 11 are indefinite under 35 U.S.C. 112, second paragraph.

3. Whether claims 1, 4-8, 12, 14-16 and 19 are unpatentable under 35 U.S.C. 103(a) over Applicant Admitted Prior Art in view of Masterson et al (U.S. 5,073,851).

4. Whether claims 2, 3, 9-11 and 13 are unpatentable under 35 U.S.C. 103(a) over Applicant Admitted Prior Art in view of Masterson et al (U.S. 5,073,851) and further in view of DeSouza et al (U.S. 5,379,289).

5. Whether claims 17 and 18 are unpatentable under 35 U.S.C. 103(a) over Applicant Admitted Prior Art in view of Masterson et al (U.S. 5,073,851) and further in view of IBM_TDB December 1979, Vol. 22, Issue No. 7, pages 2651-2654.

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ARGUMENTS FOR REPLY BRIEF

Applicant submits this reply brief for the main reason to counter the new issue raised by the Examiner in the Examiner's Answer, and to point out inaccurate assertions.

First, the Examiner states that the Appellant's statement in the brief on page 5, lines 1-4, is not disclosed in the specification.

Applicant respectfully but vigorously disagrees. The Examiner's statement here is incorrect and illustrates that the Examiner makes erroneous, incorrect assumptions and interpretations as to what Appellant is teaching and claiming, and it is respectfully submitted that this misunderstanding is what is leading to the fact the this application is on appeal.

The Examiner is misunderstanding the timing chart and the explanation. The Examiner focuses on the presence of the "READ" command at time T4/5 in the timing chart, FIG. 2, as somehow being an indication of when the data is read by the DSP chip in the invention. That is not what the timing chart is showing and that is not what Appellant has taught and argued throughout the prosecution. The READ command at time T4/5 is merely a command to set the DSP chip up for a read operation. The reading does not take place until some time slices later, WHEN THE DATA IS ACTUALLY ON THE BUS. If we are to adapt the Examiner's

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interpretation of when reads and writes occur, then somehow we would be reading data into the DSP chip before the data even appeared on the bus. We cannot read the data before it appears because it isn't there.

One specific point of the Appellant's invention is that a number of operations and steps are taken (one of which is issuing a command to the DSP chip at time T4/5) so that the DSP chip will in fact be ready to read the data when the data appears on the bus at a later time. The "READ" command at time T4/5 is separate from the actual act by the chip of reading the data. The command is what is issued to set the chip up in the particular embodiment, so that the claimed invention may be accomplished. By sending the READ command to the chip in accordance with the timing chart, the chip will then be ready at the appropriate time to read the data substantially simultaneously with the writing of the data to the memory chip.

Claim 1 recites, for example,:

> 1. A method for transferring a unit of data on a bus from a source to at least two destinations substantially simultaneously, comprising the steps of:

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supplying said unit of data from the source to first of said at least two destinations as a read data operation; and

supplying said unit of data to a second of said at least two destinations as a write operation.

Considering claim 1, note that it discusses that the unit of data is transferred to the at least 2 destinations. This is what applicant teaches. The Examiner seems to be focusing on a particular command to a chip that is in the timing chart (the "READ" command) as being the transferring of the data. But, as applicant has explained, the data transfer takes place just as claimed, when the data is present on the bus, not necessarily at the exact time of the command to the particular chip which is made during chip set up.

The Examiner says at the bottom 2 lines of page 2 of the Answer and continuing to the top 2 lines of page 3 of the Answer:

> In other words, a data W (e.g., W3) on RX_Data at a specific cycle time (i.e., T9 is written into SDRAM at said specific cycle time, but said data W (i.e., W3) is not read by DSP_Command at said specific cycle time because the reading operation was commanded (i.e., read) 2 clock cycles before said specific cycle time.

This illustrates that basic error in the position of the Examiner of what the timing chart shows and how applicant's

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invention operates. The DSP_Command line shown in the timing chart is a command signal line to the DSP chip. Data for reading is not supplied to the DSP chip on the DSP_Command line - the DSP_Command line is for sending commands to the chip. Data is provided on separate lines, which, are connected to the data bus. Still further, the timing chart shows the occurrence of events from earlier time on the left, to later time as the chart proceeds to the right. Appellant has explained before and cannot understand why we are still having to argue this point, that the data W3 (which the Examiner chooses for reference in making the Examiner's point) or any other data words Wn is not present on the data bus to be read or written at the time when the READ command is supplied to the DSP chip. We cannot read the data before it is present; we cannot know what it is until it exists. What we can do, however, and what the timing chart shows, is set up the particular chip so that it functions and operates in the manner desired and claimed, and, in the particular illustrated embodiment, that involves sending commands at earlier times, to set up the chip to operate as desired.

At page 3 of the Answer, line 8-12, the Examiner asserts the erroneous interpretation that:

> the MAC data on signal 34 is not substantially simultaneously supplied to the SDRAM and to the DSP, but the MAC data on signal 34 is supplied to the SDRAM by SDRAM Command "WRITE" at a specific cycle

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time, and other MAC data on signal 34 is supplied to the DSP by DSP Command 'READ' at 2 cycles later after said specific cycle time. (underlining in the original)

This further illustrates that the Examiner is basing the rejections on inaccuracies supplied by the Examiner, not based on any deficiency in applicant's disclosure or teachings. The data shown in the timing chart on line 34 is not supplied to the DSP chip when the DSP_Command 'READ' is given. How could it be. It isn't on the data line 34 yet. The data is supplied to the DSP chip when the data is on the bus as shown in the timing chart. The data is also supplied to the SDRAM at the same time. Both the DSP and SDRAM take their data, either as a read operation or a write operation, from the data bus line 34 in accordance with the timing shown. The Examiner is lost in focusing on timing of commands sent to the chips in order to set the chip operations up so that when the data is present on the bus, that the data is read and written substantially simultaneously to the respective chips (DSP and SDRAM). Appellant is not claiming reading/writing data to a particular chip at the exact moment that a command of some sort was sent to the chip, but the Examiner is examining the case as if that was what applicant was claiming.

This further illustrates that the rejections should not be sustained, as they are based on interpretations that are not consistent with appellant's teaching, nor with a manner of

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reading a timing chart that is well known by one of ordinary skill in the art to which the invention pertains.

The Examiner's rejections are based on the erroneous understanding of what that timing chart means.

For example, at page 4 of the Answer, the Examiner states:

> The Examiner doubts how to transfer a unit of data on a bus from a source to at least two destinations substantially simultaneously at a specific cycle time because the Appellant admits that there are 2 clock cycles latency between a read data operation and a write data operation.

As noted above, any latency (e.g. 2 cycles) is the difference between the timing of the COMMAND to the particular chips in the embodiment in their reaction to a COMMAND. Applicant does not claim that COMMANDS are sent substantially simultaneously to the chips to start their operation. Applicant is claiming that the unit of data is transferred substantially simultaneously. The COMMANDS to the chips to time their operations are not the units of data that are being supplied in the claims. So, applicant respectfully submits that the rejections are not sustainable, as they are based on erroneous assumptions and impossibilities set forth by the Examiner's arguments (such as reading data before it exists on a bus).

Other problems exist in the rejections that warrant that they not be sustained.

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For example, on page 22 of the Answer, the Examiner argues that "the actual read and write operations are not overlapped, which means said read and said write operations (i.e., data transferring) could not be substantially simultaneously performed.

Again, the Examiner's position cannot sustain a rejection. The Examiner seems throughout the prosecution and rejections to be interpreting commands sent to chips as shown on a timing chart as the same as the writing of the data to the devices with which the invention claims are concerned. But that is an erroneous interpretation. Just because in the embodiment illustrated, appellant gives a READ command to one chip at a different time from a WRITE command to another chip, does not support the Examiner's position.

On page 23 of the Answer, the Examiner states that "Appellant fails to provide any evident portion of the Examiner's statement in the record at where the above alleged issues were stated." Appellant respectfully disagrees. The whole of the Examiner's tack and statements in the prosecution and rejections, of focusing on the commands sent to chips and their timing as somehow being an admission that reading of the data takes place 2 cycles before or later than writing of the data, shows that the Examiner is stating exactly what Appellant asserts the Examiner

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is stating. Otherwise, we would not be at this point of appeal, having to be arguing about these issues. Appellant's argument on this point is not in error, and its validity is evident from inspection of the prosecution history and the positions taken by the Examiner regarding the Examiner's interpretation of the timing chart. The Examiner states at the bottom of page 4 and top of page 5 of the Answer that at a specific cycle time T9, data W3 is available on RX_Data and could be writing into SDRAM. But then, the Examiner somehow decides that the DSP chip is reading "the data W5 at said specific cycle time T9, which will be available at 2 cycles times later on the RX_data".

The timing chart of FIG. 2 does not show what the Examiner is alleging it shows. The data W3 is present on RX_Data at time slice T9 in the FIG. 2. See the figure for this information. W5 is not present at time T9. W5 does not appear until T11. This may be clearly observed by inspection of the timing chart

The Examiner's assertion of data W5 being present at time T9 is erroneous, and does not conform to what applicant shows. It doesn't fit the timing chart. It is based on some pre-set conclusion the Examiner has reached and ignores the facts and the teaching of the specification and drawings.

How can the rejection be sustained when it is based on such a position? These are things the Examiner is making up. They

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are not shown in the specification and drawings. How can applicant proceed when the Examiner is making arguments such as this that are contrary to what applicant teaches?

On page 23 of the Answer, 6 lines from the bottom of the page, the Examiner again says "the specification clearly shows said 2 clock cycles latency between said read data operation and said write data operation in Fig. 2 and Application, page 4, lines 23-24.

Again, this argument by the Examiner is not correct. The 2 cycles that the Examiner continues to focus on merely relate to the timing of sending commands to the particular chips in the particular embodiment, so that when the data appears on the bus, the chips are ready to substantially simultaneously receive the data as respective read and write operations. Page 4, lines 23-24 of the specification state that 2 clock cycles after the end of the ROW data on the Trdsp_Addr line, the Dsp_Command line is set to READ.

This portion of the specification does nothing to support the Examiner's position. The portion of the specification is merely discussing timing of different commands on different signal lines of a chip, in explaining how the operation is accomplished in the illustrated embodiment. Even if the Examiner's position was somehow valid, the referred to portion of

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the specification by the Examiner does nothing to support the Examiner's position. It is merely discussing that 2 cycles after a command signal on one particular line ("the end of the ROW data on the Trdsp_Addr line), another command signal is given. It has nothing to do with support of the Examiner's position.

Appellant stands on the brief submitted previously, with the addition of the above comments and arguments as to points newly raised by the Examiner in the Answer.

It is respectfully requested that the rejections be overturned and that the claims be allowed.

Respectfully submitted,

James H. Walters, Reg. No. 35,731

Customer number 802
Dellett and Walters
P.O. Box 2786
Portland, OR 97208-2786
(503) 224-0115
F-316

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